Product List

SM59364C25, 25MHz 64KB internal flash MCU
SM59364C40, 40MHz 64KB internal flash MCU

Description

The SM59364 series product is an 8 - bit single chip micro controller with 64KB flash & 1K byte RAM embedded. It has In-System Programming (ISP) function and is a derivative of the 8052 micro controller family. With its hardware features and powerful instruction set, it's straight forward to make it a versatile and cost effective controller for those applications which demand up to 24 I/O pins for PLCC package, or applications which need up to 64K byte flash memory either for program or for data or mixed. The on-chip flash memory can be programmed in either parallel or serial interface with its ISP feature.

Features

- Working Voltage:4.5V through 5.5V
- General 8052 family compatible
- 12 clocks per machine cycle
- 64K byte on chip program flash with in-System Programming(ISP) capability
- 1024 bytes on chip data RAM
- Three 16 bit Timers/Counters
- One Watch Dog Timer
- Three 8-bit I/O ports-for PLCC-package
- Full duplex serial channel
- Bit operation instruction
- Industrial Level
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes: Idle mode and Power down mode
- Code protection function
- Low EMI (inhibit ALE)
- Reset with address $0000 blank initiate ISP service program

Ordering Information

yymmv
SM59364ihhkL

yy: year, mm: month
v: version identifier{ , A, B,…}
i: process identifier {L=3.0V~3.6V,C=4.5V~ 5.5V}
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}
L:PB Free identifier
{No text is Non-PB Free，" P" is PB Free}

Postfix	Package	Pin / Pad Configuration	Dimension
H	32L PLCC	Page 2	Page 19

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TEL: 886-3-567-1820
886-3-567-1880
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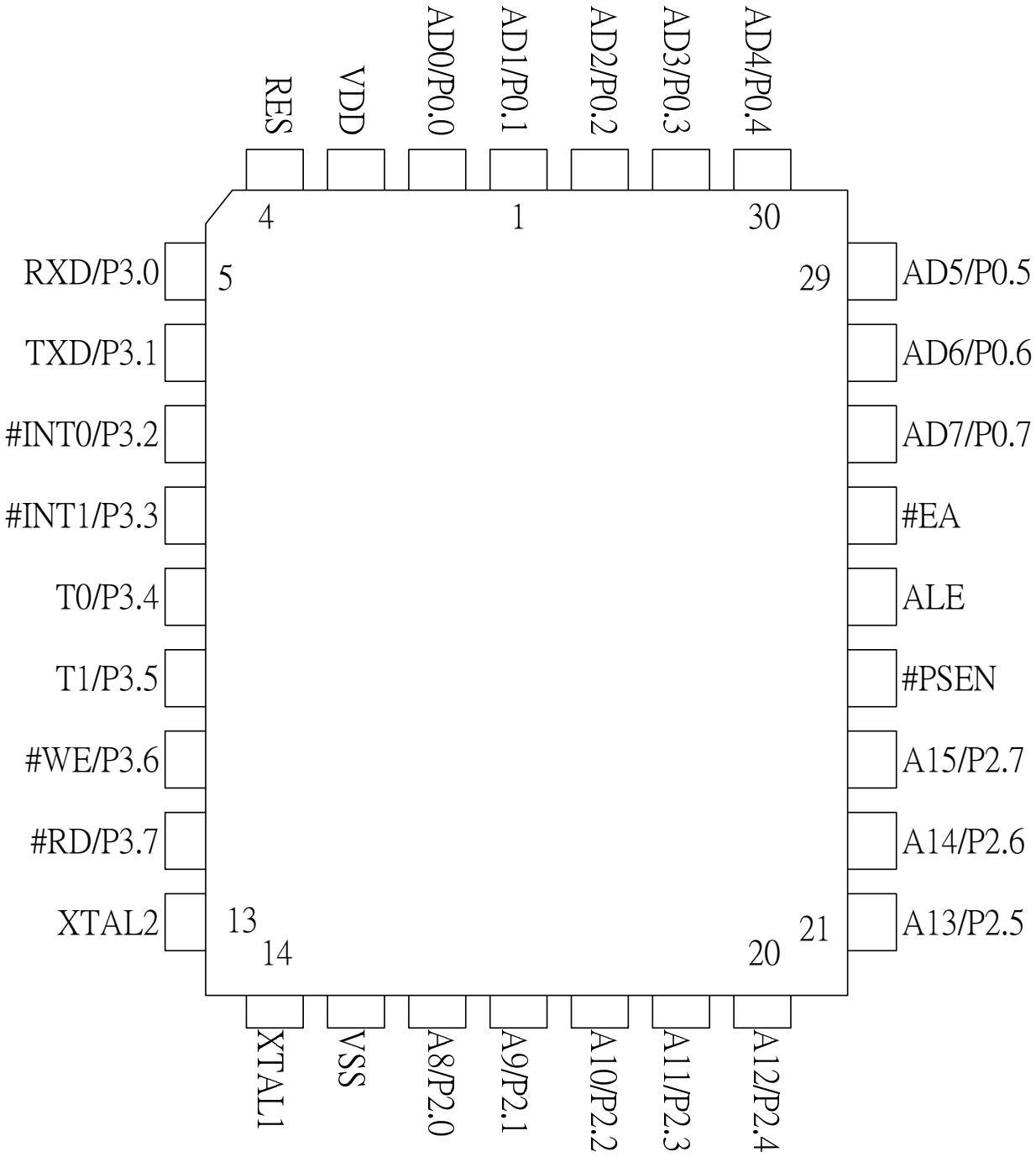
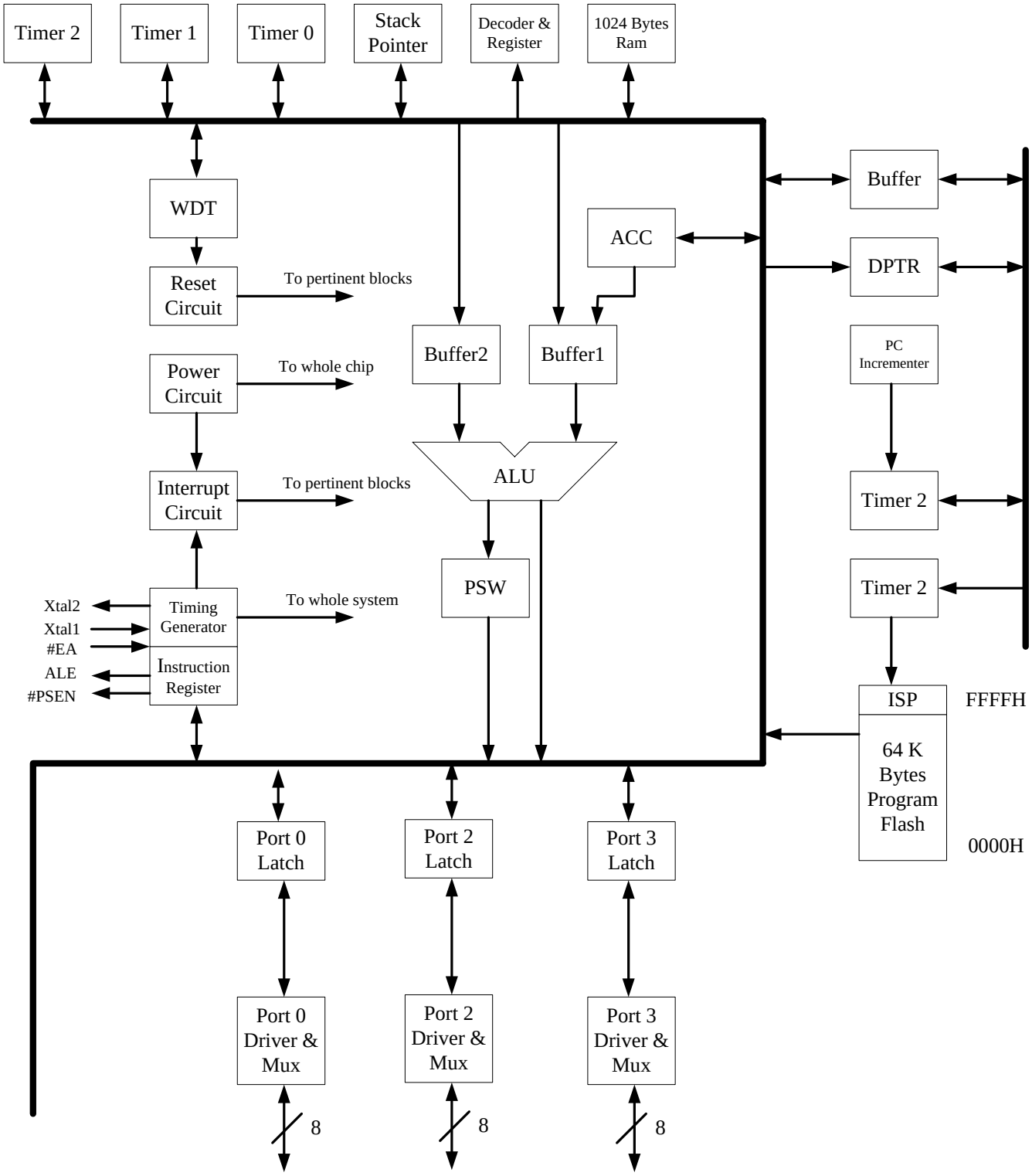
Pin Configuration



Block Diagram



Pin Description

32L PLCC Pin#	Symbol	Active	I/O	Names
4	RES	H	i	Reset
5	P3.0/RXD		i/o	bit 0 of port 3 & Receiver data
6	P3.1/TXD		i/o	bit 1 of port 3 & Transmit data
7	P3.2/#INT0	L/-	i/o	bit 2 of port 3 & low true interrupt 0
8	P3.3/#INT1	L/-	i/o	bit 3 of port 3 & low true interrupt 1
9	P3.4/T0		i/o	bit 4 of port 3 & Timer 0
10	P3.5/T1		i/o	bit 5 of port 3 & Timer 1
11	P3.6/#WR		i/o	bit 6 of port 3 & ext. memory write
12	P3.7/#RD		i/o	bit 7 of port 3 & ext. memory read
13	XTAL2		o	Crystal out
14	XTAL1		i	Crystal in
15	VSS			Sink Voltage, Ground
16	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of ext. memory address
17	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of ext. memory address
18	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of ext. memory address
19	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of ext. memory address
20	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of ext. memory address
21	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of ext. memory address
22	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of ext. memory address
23	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of ext. memory address
24	#PSEN	L	o	program storage enable
25	ALE	-	o	address latch enable
26	#EA	L	I	external access
27	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of ext. memory
28	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of ext. memory
29	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of ext. memory
30	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of ext. memory
31	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of ext. memory
32	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of ext. memory
1	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of ext. memory
2	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of ext. memory
3	VDD			Drive Voltage

Special Function Register (SFR)

The address $80 to $FF can be accessed by direct addressing mode only.
Address $80 to $FF is SFR area.
The following table lists the SFRs which are identical to general 8052 as well as SM59364 Extension SFRs .

Special Function Register (SFR) Memory Map

$F8									$FF
$F0	B				**ISPFAH**	**ISPFAL**	**ISPFD**	**ISPC**	$F7
$E8									$EF
$E0	ACC								$E7
$D8									$DF
$D0	PSW								$D7
$C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			$CF
$C0									$C7
$B8	IP							**SCONF**	$BF
$B0	P3								$B7
$A8	IE								$AF
$A0	P2								$A7
$98	SCON	SBUF						**WDTC**	$9F
$90									$97
$88	TCON	TMOD	TL0	TL1	TH0	TH1			$8F
$80	P0	SP	DPL	DPH		**RCON**		PCON	$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM59364

Addr	SFR	Reset	7	6	5	4	3	2	1	0
85H	**RCON**	******00							RAMS1	RAMS0
9FH	**WDTC**	0*0**000	WDTE	Reserved**	CLEAR			PS2	PS1	PS0
BFH	**SCONF**	0****010	WDR					ISPE	OME	ALEI
C9H	**T2MOD**	******00	*	*	*	*	*	*	T2OE	DCEN
D8H	**P4**	****1111					P4.3	P4.2	P4.1	P4.0
F4H	**ISPFAH**	00H	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
F5H	**ISPFAL**	00H	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
F6H	**ISPFD**	00H	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
F7H	**ISPC**	0*****00	START						F1	F0

** Keep to “0” when write WDTC (9FH).

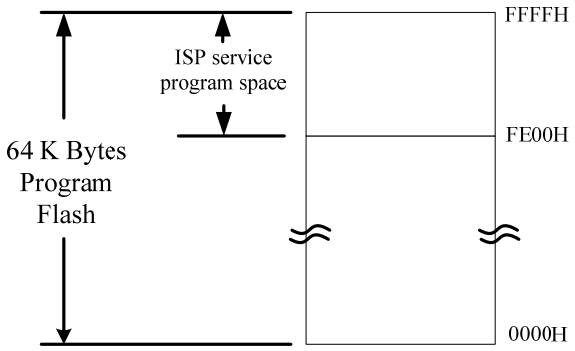
Extension Function Description

1. Memory Structure

The SM59364 is the general 8052 hardware core to integrate the ISP function as a single chip micro controller. It’s memory structure follows general 8052 structure .

1.1 Program Memory

The SM59364 has 64K byte on-chip flash memory which used as general program memory, on which include 512 byte specific ISP service program memory space. The address range for the 64K byte is $0000 to $FFFF. The address range for the ISP service program is $FE00 to $FFFF.

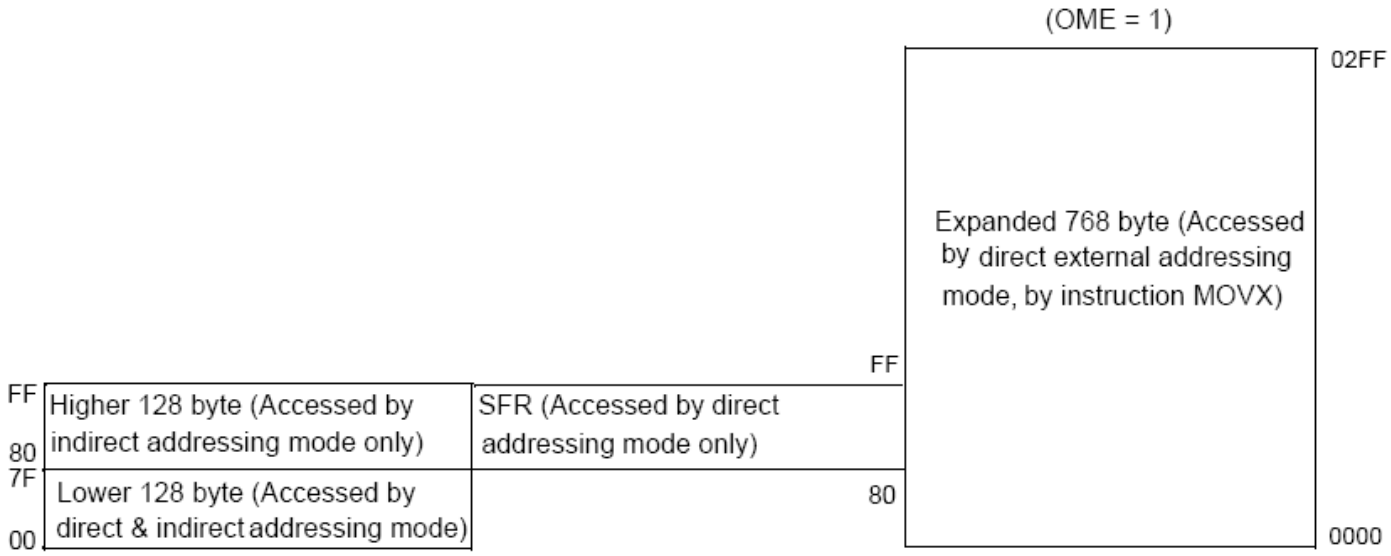


1.1.1 Program Code Security

MOVC instruction executed from external program memory space will not be able to fetch internal codes from on chip program memory after the chip is protected on the Writer.

1.2 Data Memory

The SM59364 has 1K bytes on-chip RAM, 256 bytes of it are the same as general 8052 internal memory structure while the expanded 768 bytes on-chip RAM can be accessed by external memory addressing method (by instruction MOVX.).



1.2.1 Data Memory - Lower 128 byte ($00 to $7F)

Data Memory $00 to $FF is the same as 8052.

The address $00 to $7F can be accessed by direct and indirect addressing modes.

Address $00 to $1F is register area.

Address $20 to $2F is memory bit area.

Address $30 to $7F is for general memory area.

1.2.2 Data Memory - Higher 128 byte ($80 to $FF)

The address $80 to $FF can be accessed by indirect addressing mode .

Address $80 to $FF is data area.

1.2.3 Data Memory - Expanded 768 bytes ($0000 to $02FF)

From external address $0000 to $02FF is the on-chip expanded RAM area, total 768 bytes. This area can be accessed by external direct addressing mode (by instruction MOVX).

If the address of instruction MOVX @DPTR is larger than $02FF then SM59364 will generate the external memory control signal automatically. The bit 1 (OME) of special function register $BF (SCONF) can enable or disable this expanded 768 byte RAM. The default setting of OME bit is 1 (enable).

System Control Register (SCONF, $BF)

bit-7 bit-0

	WDR	Unused	Unused	Unused	DFEN	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	*	*	*	0	1	0

WDR: Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1.
ISPE: ISP function enable bit
OME: 768 bytes on-chip RAM enable bit .
ALEI: ALE output inhibit bit, to reduce EMI .

Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.
The bit 1 (OME) of SCONF can enable or disable the on-chip expanded 768 byte RAM. The default setting of OME bit is 1 (enable).
The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

2. In-System Programming (ISP) Function

The SM59364 can generate flash control signal by internal hardware circuit. User utilize flash control register, flash address register and flash data register to perform the ISP function without removing the SM59364 from the system.

The SM59364 provides internal flash control signals which can do flash program/chip erase/page erase/protect functions. User need to design and use any kind of interface which SM59364 can input data. User then utilize ISP service program to perform the flash program/chip erase/page erase/protect functions.

2.1 ISP Service Program

The ISP service program is a user developed firmware program which resides in the ISP service program space. After user developed the ISP service program, user then determine the size of the ISP service program. User need to program the ISP service program in the SM59364 for the ISP purpose.

The ISP service program were developed by user so that it should includes any features which relates to the flash memory programming function as well as communication protocol between SM59364 and host device which output data to the SM59364. For example, if user utilize UART interface to receive/transmit data between SM59364 and host

device, the ISP service program should include baud rate, checksum or parity check or any error-checking mechanism to avoid data transmission error.

The ISP service program can be initiated under SM59364 active or idle mode. It can not be initiated under power down mode.

2.2 Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are two ways to do so:
(1) Blank reset. Hardware reset with first flash address blank ($0000=#FFH) will load the PC with start address of ISP service program.
(2) Execute 'JUMP' instruction can load the start address of the ISP service program to PC.

User can initiate general 8052 INT function to initiate the ISP service program. After ISP service program executed, user need to reset the SM59364, either by hardware reset or by WDT, or jump to the address $0000 to re-start the firmware program.

ISP Registers - ISPFAH, ISPFAL, ISPFD and ISPC

ISP Flash Address-High Register(ISPFAH,$F4)

	bit-7							bit-0
	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA15 ~ FA8: flash address-high for ISP function

ISP Flash Address-Low Register(ISPFAL,$F5)

	bit-7							bit-0
	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA7 ~ FA0: flash address-low for ISP function

The ISPFAH & ISPFAL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPFAH & ISPFAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

ISP Flash Data Register (ISPFD, $F6)

	bit-7							bit-0
	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FD7 ~FD0 : flash data for ISP function

The ISPFD provide the 8-bit data for ISP function

ISP Flash Control Register (ISPC, $F7)

	bit-7							bit-0
	START	Unused	Unused	Unused	Unused	Unused	ISPF1	ISPF0
Read / Write:	R/W	-	-	-	-	-	R/W	R/W
Reset value:	0	*	*	*	*	*	0	0

F[1: 0]: ISP function select bit
START: ISP function start bit
= 1: start ISP function which indicated by bit 1, bit 0 (F1, F0)
= 0: no operation

The START bit is read-only by default, software must write three specific values 55H, AAH and 55H sequentially to the ISPFD register to enable the START bit write attribute. That is:

```
MOV ISPFD, #55H
MOV ISPFD, #0AAH
MOV ISPFD, #55H
```

Any attempt to set START bit will not be allowed without the procedure above.

After START bit set to 1 then the SM59364 hardware circuit will latch address and data bus and hold the program counter until the START bit reset to 0 when ISP function finished. User does not need to check START bit status by software method.

F[1:0]	ISP function
00	Byte program
01	Chip protect
10	Page erase
11	Chip erase

F[1:0]: ISP function select bit

One page of flash memory is 512 byte.

To perform byte program/page erase ISP function, user need to specify flash address at first. When performing page erase function, SM59364 will erase entire page which flash address indicated by ISPFAH & ISPFAL registers located within the page.

e.g. flash address: $XYMN

page erase function will erase from $XY00 to $X(Y+1)FF (Y:even number), or
page erase function will erase from $X(Y-1) 00 to $XYFF (Y:odd number)

To perform the chip erase ISP function, SM59364 will erase all the flash program memory except the ISP service program space, also, SM59364 will un-protect the flash memory automatically. To perform chip protect ISP function, the SM59364 flash memory content will be read #00H.

e.g. ISP service program to do the byte program - to program #22H to the address $1005H

```
MOV SCONF,#04H      ; enable SM59364 ISP function
MOV ISPFAH,#10H     ; set flash address-high, 10H
MOV ISPFAL,#05H     ; set flash address-low, 05H
MOV ISPFD,#22H      ; set flash data to be programmed, data = 22H
MOV ISPC,#80H       ; start to program #22H to the flash address $1005H
                    ; after byte program finished, START bit of ISPC will be reset to 0 automatically
                    ; program counter then point to the next instruction
```

ISP Registers - System Control Register (SCONF,$BF)

	bit-7							bit-0
	WDR	Unused	Unused	Unused	Unused	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	*	*	*	0	1	0

The bit 2 (ISPE) of SCONF is ISP enable bit. User can enable overall SM59364 ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0.

The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally.

3. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover form abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDR bit of SCONF register whenever un-predicted reset happened

The WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) of Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the selected time base source clock which set by PS2~PS0. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM59364 been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the CLEAR bit of WDTC. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

3.1 Watch Dog Timer Registers: WDTC and SCONF

Watch Dog Timer Registers - WDT Control Register (WDTC, $9F)

bit-7 bit-0

	WDTE	reserved**	Clear	Unused	Unused	PS2	PS1	PS0
Read / Write:	R/W	-	R/W	-	-	R/W	R/W	R/W
Reset value:	0	*	0	*	*	0	0	0

** Keep to “0” when write WDTC (9FH).

WDTE : Watch Dog Timer enable bit
CLEAR : Watch Dog Timer reset bit
PS[2:0] : Overflow period select bits

PS [2:0]	Divider(OSC in)	Time Period (ms) @ 40 MHZ
000	8	13.12.048
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

Watch Dog Timer Register - System Control Register (SCONF, $BF)

bit-7 bit-0

	WDR	Unused	Unused	Unused	Unused	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	*	*	*	0	1	0

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

4. Reduce EMI Function

The SM59364 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin.

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 25	Oscillator Frequency	3.0	25	25	MHz	For 5V application
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

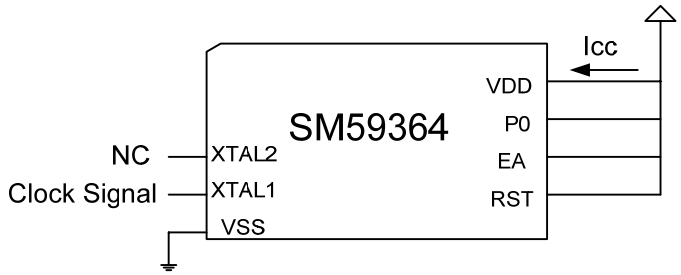
DC Characteristics

(TA = -40 degree C to 85 degree C, Vcc = 5.5V)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,2,3,4,#EA	-0.5	0.8	V	Vcc=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High Voltage	port 0,2,3,4,#EA	2.0	Vcc+0.5	V	
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		±10	uA	0.45V<Vin<Vcc
R RES	Reset Pull-down Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25 ℃
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

Note1:Under steady state (non-transient) conditions, IOL must be externally
Limited as follows : Maximum IOL per port pin : 10mA
Maximum IOL per 8-bit port : port 0 :26mA
port 2,3 :15mA
Maximum total IOL for all output pins : 71mA
If IOL exceeds the condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

Icc Active Mode Test Circuit



AC Characteristics

(16/25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=150pF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT-10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT-10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT -20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT+20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT-10		3xT+10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT-20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT-35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

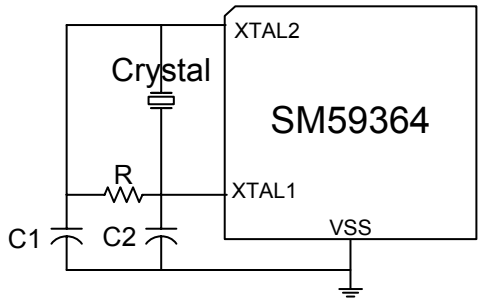
ISP Test Conditions

(40 MHZ, typical operating conditions, valid for SM59364 series)

Symbol	MAX	Remark
Chip erase	3000ms	Vcc = 5V
Page erase	10ms	"
Program	30us	"
Protect	400us	"

Application Reference

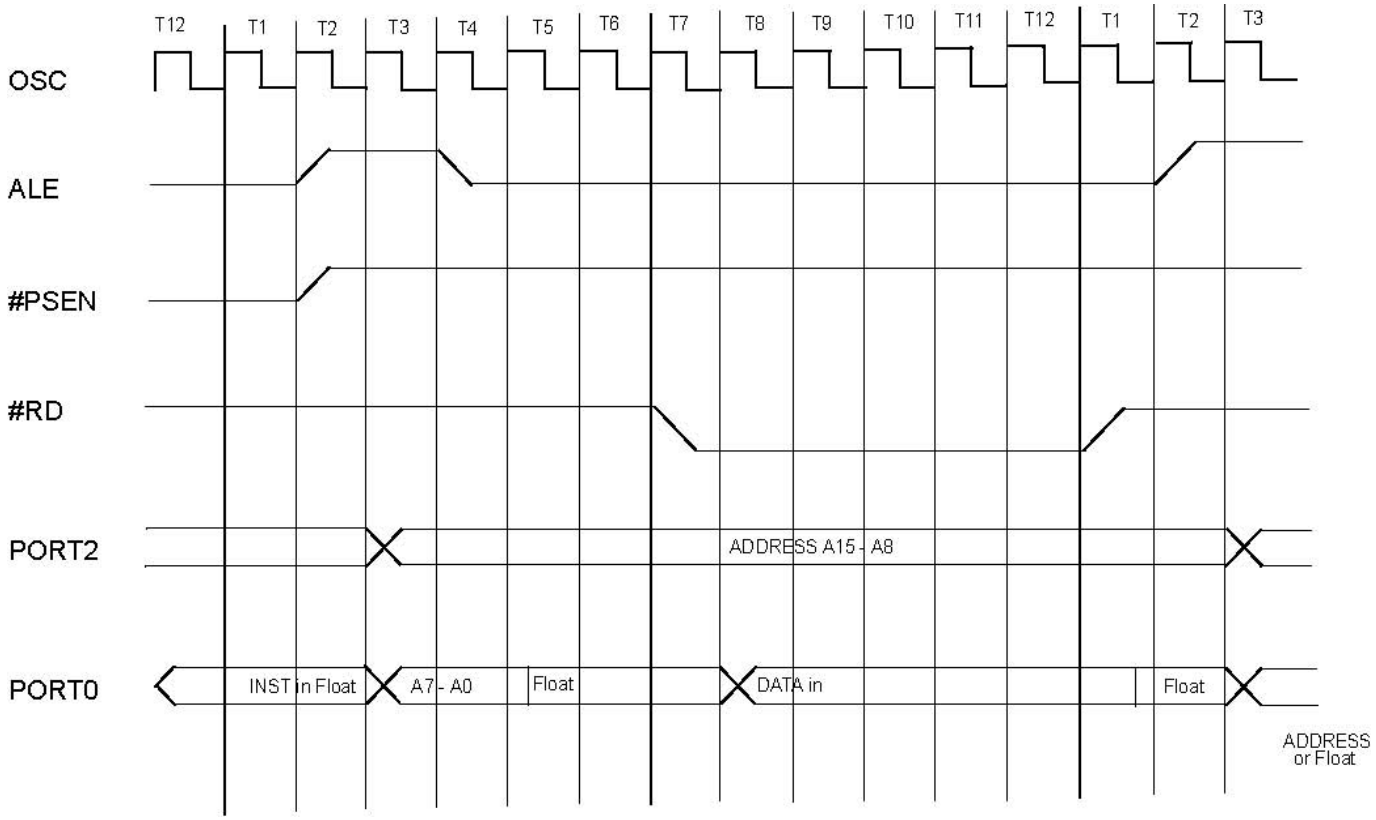
Valid for SM59364				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	5 pF	2 pF
C2	30 pF	15 pF	5 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ



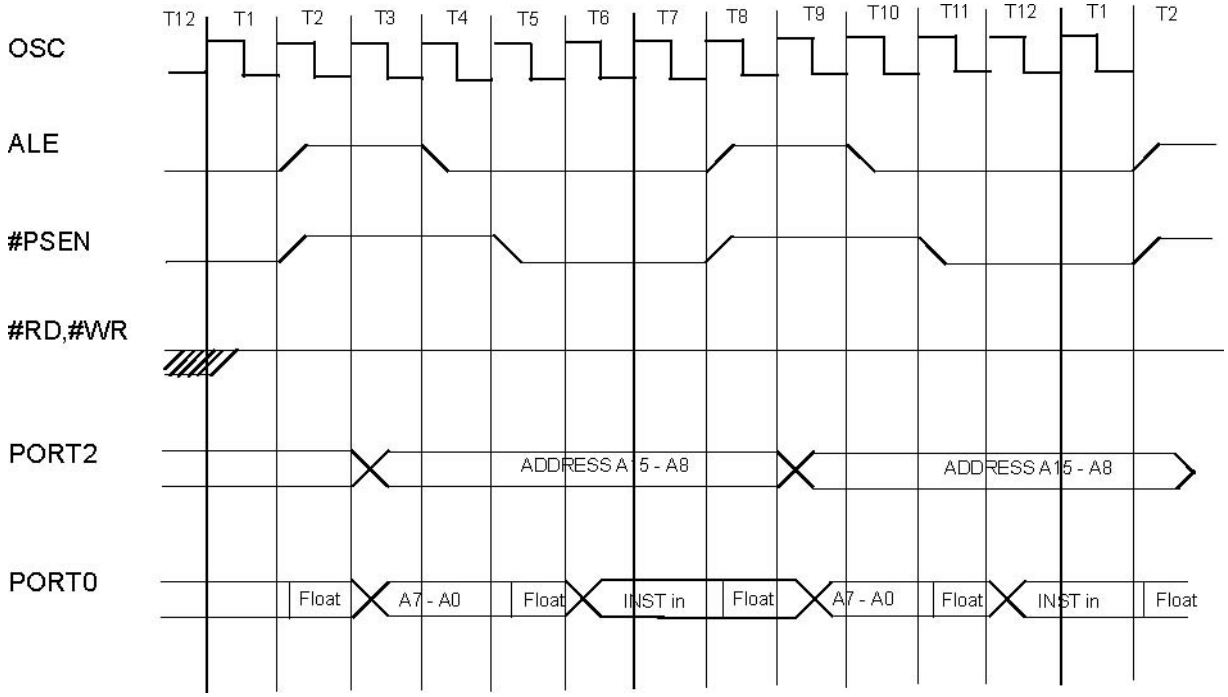
NOTE: Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics.

User should check with the crystal or ceramic resonator manufacture for appropriate value of external components.

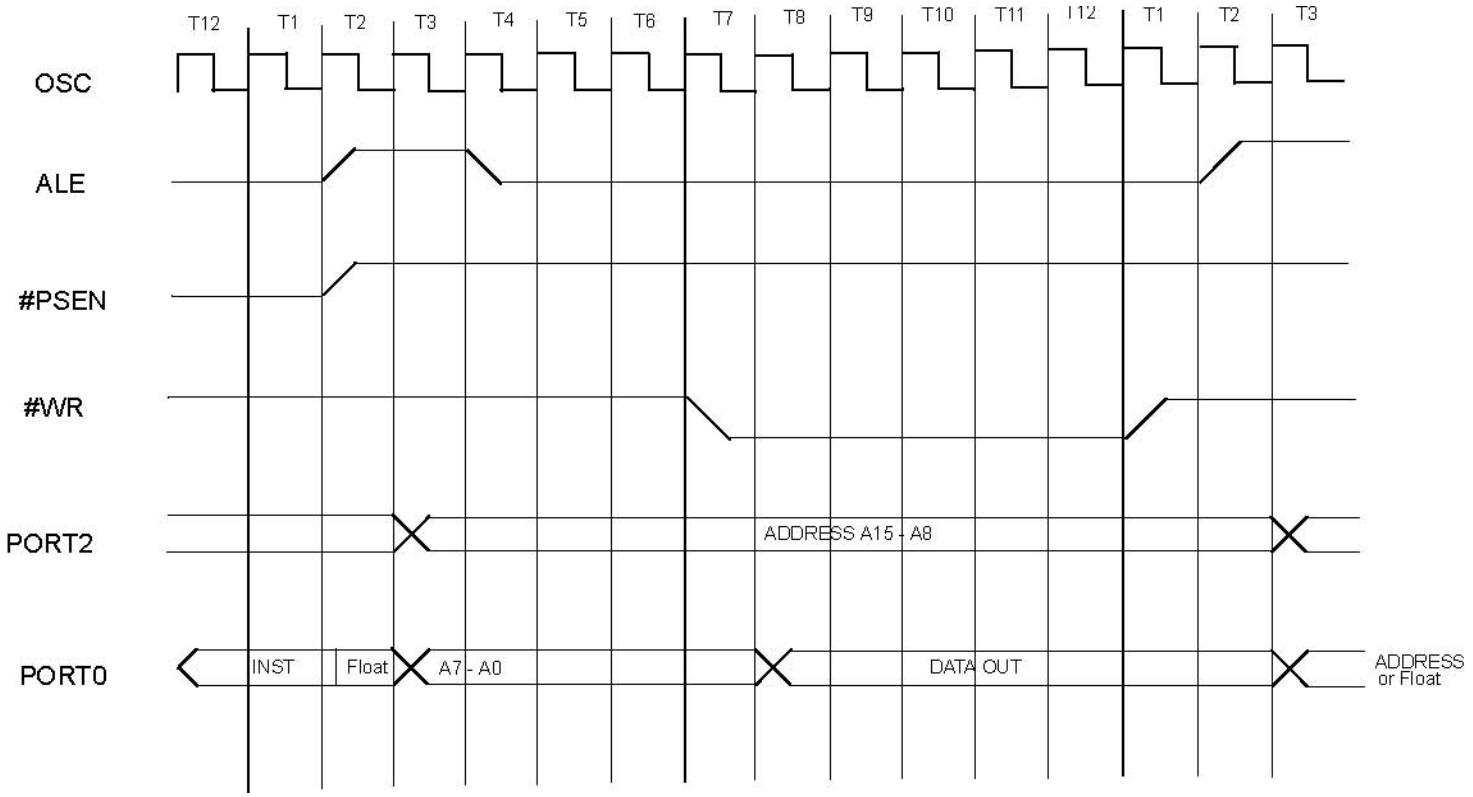
Data Memory Read Cycle Timing



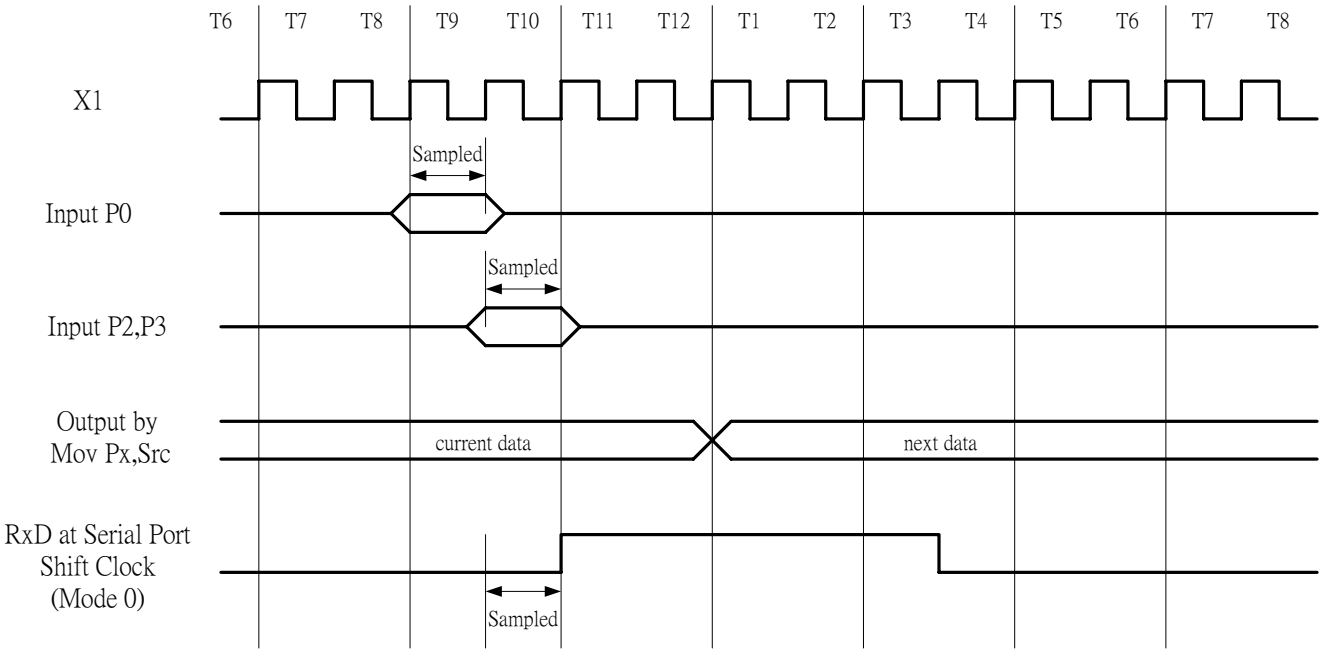
Program Memory Read Cycle Timing



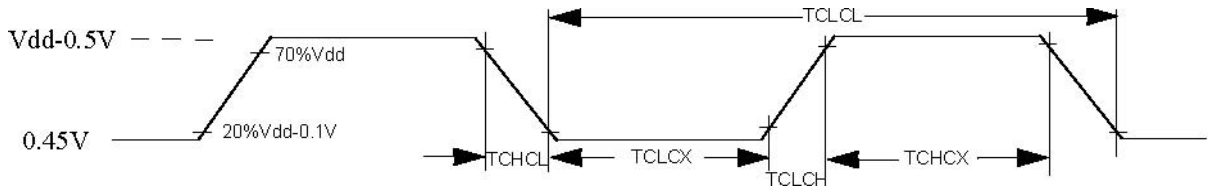
Data Memory Write Cycle Timing



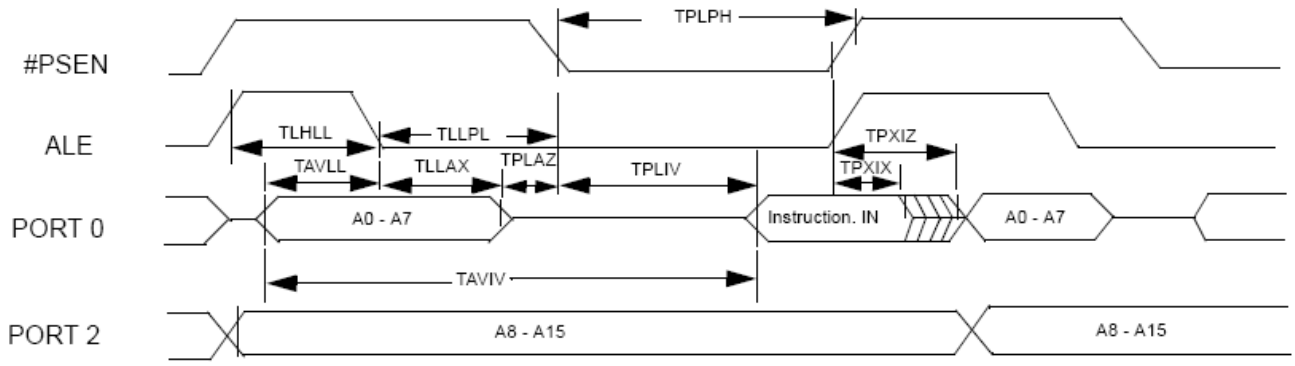
I/O Ports Timing



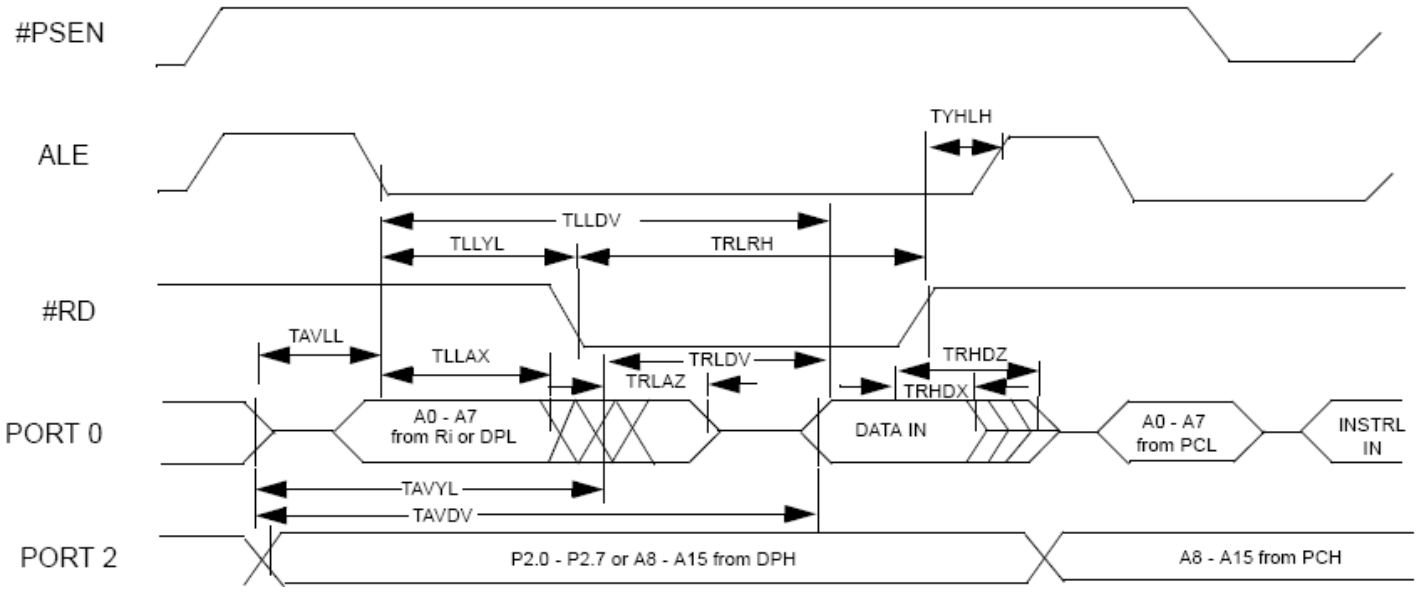
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



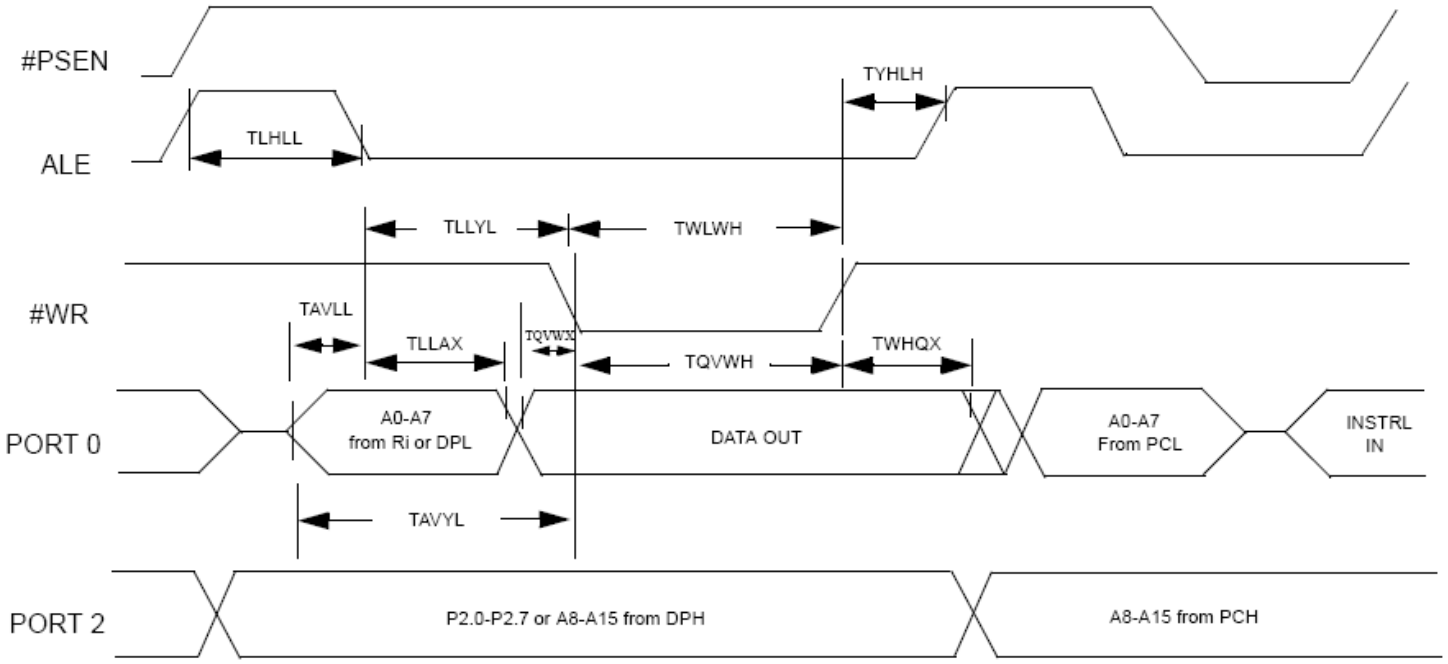
Tm.I External Program Memory Read Cycle



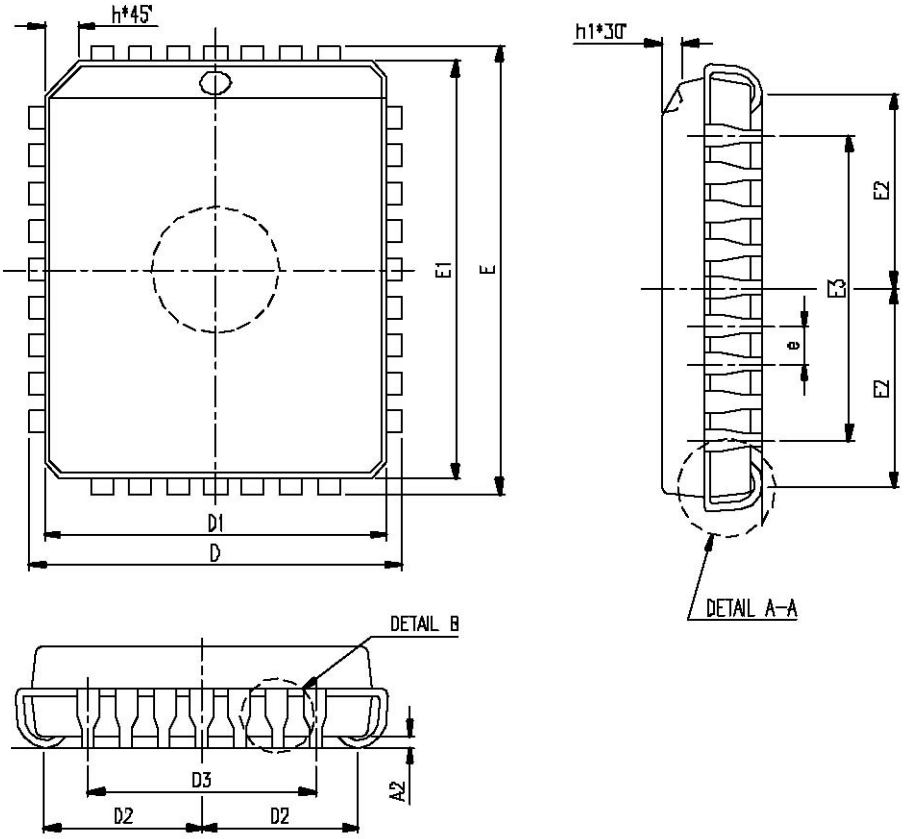
Tm.II External Data Memory Read Cycle

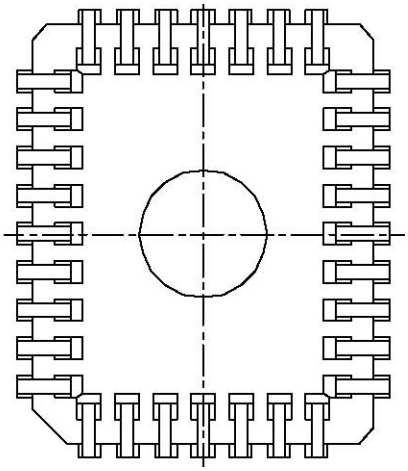


Tm.III External Data Memory Write Cycle



PLCC 32L Package Information：





SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	3.18	3.55	0.125	0.140
A1	1.53	2.41	0.060	0.095
A2	0.38		0.015	
D	12.32	12.57	0.485	0.495
D1	11.36	11.50	0.447	0.453
D2	4.78	5.66	0.188	0.223
D3	7.62 BSC		0.300 BSC	
e	1.27 BSC		0.050 BSC	
E	14.86	15.11	0.585	0.595
E1	13.90	14.04	0.547	0.553
E2	6.05	6.93	0.238	0.273
E3	10.16 BSC		0.400 BSC	
c	0.254 BSC		0.010 BSC	
b1	0.66	0.82	0.026	0.032
b2	0.33	0.54	0.013	0.021
h	1.060	1.220	0.042	0.048
h1	0.58	0.74	0.023	0.029
JEDEC	MS-016 (AE)			