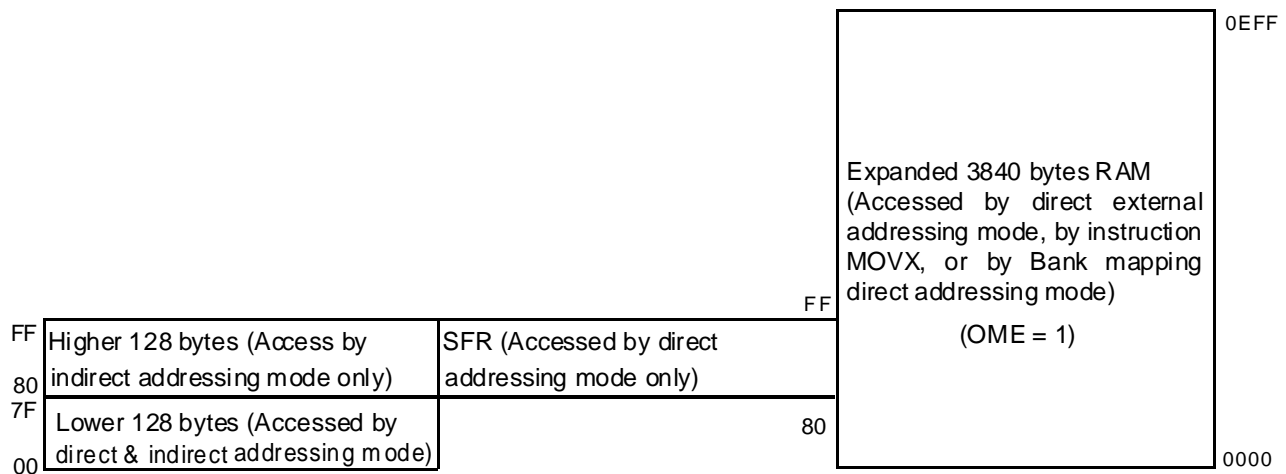




Expanded RAM Application Note

Data Memory

- The SM79164 has 4K bytes on-chip RAM, 256 bytes of it are the same as general 8052 internal memory structure while the expanded 3840 bytes on-chip RAM can be accessed by external memory addressing method (by instruction MOVX), or by 'Bank mapping direct addressing mode' as described in page 8.



On-chip expanded RAM address structure.

Data Memory - Lower 128 byte (\$00 to \$7F, Bank 0 & Bank 1)

Data Memory \$00 to \$FF is the same as 8052.

The address \$00 to \$7F can be accessed by direct and indirect addressing modes.

Address \$00 to \$1F is register area.

Address \$20 to \$2F is memory bit area.

Address \$30 to \$7F is for general memory area.

Data Memory - Higher 128 byte (\$80 to \$FF, Bank 2 & Bank 3)

The address \$80 to \$FF can be accessed by indirect addressing mode or by bank mapping direct addressing mode.

Address \$80 to \$FF is data area.



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Data Memory - Expanded 3840 bytes (\$0000 to \$0EFF, Bank 4 ~ Bank 63)

From external address \$0000 to \$0EFF is the on-chip expanded RAM area, total 3840 bytes. This area can be accessed by external direct addressing mode (by instruction MOVX) or by bank mapping direct addressing mode as described below:

Bank mapping direct addressing mode:

We provide RAM bank address '40H~7FH' as mapping window which allow user access all the 4KB on-chip RAM through this RAM bank address.

That means using direct addressing mode can access all the 4KB on-chip RAM. Please see next page for the mapping mode table.

| BS5 | BS4 | BS3 | BS2 | BS1 | BS0 | 040h~07fh mapping address | Note |
|-----|-----|-----|-----|-----|-----|---------------------------|--------------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 000h~03fh | lower 128 byte RAM |
| 0 | 0 | 0 | 0 | 0 | 1 | 040h~07fh | lower 128 byte RAM |
| 0 | 0 | 0 | 0 | 1 | 0 | 080h~0bfh | higher 128 byte RAM |
| 0 | 0 | 0 | 0 | 1 | 1 | 0c0h~0ffh | higher 128 byte RAM |
| 0 | 0 | 0 | 1 | 0 | 0 | 0000h~003fh | on-chip expanded 3840 byte RAM |
| 0 | 0 | 0 | 1 | 0 | 1 | 0040h~007fh | " |
| 0 | 0 | 0 | 1 | 1 | 0 | 0080h~00bfh | " |
| 0 | 0 | 0 | 1 | 1 | 1 | 00c0h~00ffh | " |
| 0 | 0 | 1 | 0 | 0 | 0 | 0100h~013fh | " |
| 0 | 0 | 1 | 0 | 0 | 1 | 0140h~017fh | " |
| 0 | 0 | 1 | 0 | 1 | 0 | 0180h~01bfh | " |
| 0 | 0 | 1 | 0 | 1 | 1 | 01c0h~01ffh | " |
| 0 | 0 | 1 | 1 | 0 | 0 | 0200h~023fh | " |
| 0 | 0 | 1 | 1 | 0 | 1 | 0240h~027fh | " |
| 0 | 0 | 1 | 1 | 1 | 0 | 0280h~02bfh | " |
| 0 | 0 | 1 | 1 | 1 | 1 | 02c0h~02ffh | " |
| 0 | 1 | 0 | 0 | 0 | 0 | 0300h ~ 033fh | " |
| 0 | 1 | 0 | 0 | 0 | 1 | 0340h ~ 037fh | " |
| 0 | 1 | 0 | 0 | 1 | 0 | 0380h ~ 03bfh | " |
| 0 | 1 | 0 | 0 | 1 | 1 | 03c0h ~ 03ffh | " |
| 0 | 1 | 0 | 1 | 0 | 0 | 0400h ~ 043fh | " |
| 0 | 1 | 0 | 1 | 0 | 1 | 0440h ~ 047fh | " |
| 0 | 1 | 0 | 1 | 1 | 0 | 0480h ~ 04bfh | " |
| 0 | 1 | 0 | 1 | 1 | 1 | 04c0h~04ffh | " |
| ~ | ~ | ~ | ~ | ~ | ~ | ~ | ~ |
| 1 | 1 | 1 | 0 | 0 | 1 | 0d40h ~ 0d7fh | " |
| 1 | 1 | 1 | 0 | 1 | 0 | 0d80h ~ 0dbfh | " |
| 1 | 1 | 1 | 0 | 1 | 1 | 0dc0h ~ 0dffh | " |
| 1 | 1 | 1 | 1 | 0 | 0 | 0e00h ~ 0e3fh | " |
| 1 | 1 | 1 | 1 | 0 | 1 | 0e40h ~ 0e7fh | " |
| 1 | 1 | 1 | 1 | 1 | 0 | 0e80h ~ 0ebfh | " |
| 1 | 1 | 1 | 1 | 1 | 1 | 0ec0h ~ 0effh | " |

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With this bank mapping scheme, user can access entire 4k byte on-chip RAM with direct addressing method. That means using the window area (\$040~\$07F), user can access any bank (64 byte) data of 4k byte on-chip RAM space which is selected by BS[5:0] of data bank control register (DBANK, \$86).

For example, user write #30h to \$101 address:

```
MOV    DBANK, #88H      ; set bank mapping $040~$07f to $0100~$013f
MOV    A, #30H         ; store #30H to A
MOV    41H, A          ; write #30H to $0101 address
```

Data Bank Control Register (DBANK, \$86)

| | | bit-7 | | | | bit-0 | | | |
|---------------|--|-------|--------|-----|-----|-------|-----|-----|-----|
| | | BSE | Unused | SB5 | SB4 | SB3 | SB2 | SB1 | SB0 |
| Read / Write: | | R/W | - | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: | | 0 | * | 0 | 0 | 0 | 0 | 0 | 1 |

Data bank select enable bit BSE = 1 enables the data bank select function

Data bank select enable bit BSE = 0 disables the data bank select function

BS[5:0] setting will map \$040~\$07F RAM space to entire 4K byte on-chip RAM space.

Internal RAM Control Register (RCON, \$85)

| | | bit-7 | | | | bit-0 | | | |
|---------------|--|--------|--------|--------|--------|-------|-------|-------|-------|
| | | Unused | Unused | Unused | Unused | RAMS3 | RAMS2 | RAMS1 | RAMS0 |
| Read / Write: | | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset value: | | * | * | * | * | 0 | 0 | 0 | 0 |

SM79164 has 3840 byte on-chip RAM which can be accessed by external memory addressing method only. (By instruction MOVX). The address space of instruction MOVX @Rn is determined by bit 3, bit2, bit1, bit 0 (RAMS3, RAMS2, RAMS1, RAMS0) of RCON. The default setting of RAMS3, RAMS2, RAMS1, RAMS0 bits is 0000 (page0).

| RAMS3 | RAMS2 | RAMS1 | RAMS0 | MOVX @Ri i=0,1 mapping to expended RAM address |
|-------|-------|-------|-------|--|
| 0 | 0 | 0 | 0 | \$0000 ~ \$00FF |
| 0 | 0 | 0 | 1 | \$0100 ~ \$01FF |
| 0 | 0 | 1 | 0 | \$0200 ~ \$02FF |
| 0 | 0 | 1 | 1 | \$0300 ~ \$03FF |
| 0 | 1 | 0 | 0 | \$0400 ~ \$04FF |
| 0 | 1 | 0 | 1 | \$0500 ~ \$05FF |
| 0 | 1 | 1 | 0 | \$0600 ~ \$06FF |
| 0 | 1 | 1 | 1 | \$0700 ~ \$07FF |

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| | | | | |
|---|---|---|---|-----------------|
| 1 | 0 | 0 | 0 | \$0800 ~ \$08FF |
| 1 | 0 | 0 | 1 | \$0900 ~ \$09FF |
| 1 | 0 | 1 | 0 | \$0A00 ~ \$0AFF |
| 1 | 0 | 1 | 1 | \$0B00 ~ \$0BFF |
| 1 | 1 | 0 | 0 | \$0C00 ~ \$0CFF |
| 1 | 1 | 0 | 1 | \$0D00 ~ \$0DFF |
| 1 | 1 | 1 | 0 | \$0E00 ~ \$0EFF |

The port 0, port2, port3.6 and port3.7 can be used as general purpose I/O pin while port0 is open-drain structure.

System Control Register (SCONF,\$BF)

| | Bit-7 | | | | | bit-0 | |
|---------------|-------|--------|--------|--------|--------|-------|------|
| | WDR | Unused | Unused | Unused | Unused | OME | ALEI |
| Read / Write: | R/W | - | - | - | - | R/W | R/W |
| Reset value: | 0 | * | * | * | * | 0 | 0 |

OME : 3840 bytes on-chip RAM enable bit. The bit 0 (OME) of SCONF can enable or disable the on-chip expanded 3840 Byte RAM. The default setting of OME bit is 0 (disable).

Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.

The bit 1 (OME) of SCONF can enable or disable the on-chip expanded 3840 byte RAM. The default setting of OME bit is 0 (disable).

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

I/O ports status when using MOVX instruction

Intel 80C52 uses port 0 & port 2 as address bus and uses port 0 as data bus for external memory address.

In normal operation of using MOVX instruction to access external memory, 80C52 will output the address signal onto port 0 and port 2 and then input or output data through port 0.

While 80C52 output (write) data to external memory through port 0,through port 0,the #WR (P3.6) pin will be active accordingly.

e.g. write instruction MOVX @Ri, A
or MOVX @DPTR, A



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Similarly, while 80C52 input (read) data from external memory through port 0, the #RD (P3.7) signal will be active accordingly.

e.g. write instruction MOVX A, @Ri
or MOVX A, @DPTR

SM79164 follows the above described original Intel 80C52 I/O port structure: port 0 is open drain, port 1, port 2 & port 3 are general purpose I/O. The extra port 4 of SM79164 is also a general purpose I/O.

SM79164 users need to follow below guidelines for MOVX instruction.

If RAM address > 0EFFH

Meaning SM79164 accessing off-chip external memory by MOVX instruction, the corresponding port 0, port 2, #WR/P3.6 & #RD/P3.7 signals will behave the same as above described 80C52 Input/Output pins.

If 0 < RAM address < 0EFFH

Meaning SM79164 accessing off-chip external memory by MOVX instruction,

The port 0 will function as input port only.

The port 2 can be used as general purpose I/O.

The #WR/P3.6 can be used as general purpose I/O.

The #RD/P3.7 can be used as general purpose I/O.